Claims

[c1] 1. A method of fabricating a structure, comprising:

(a) providing a substrate;

(b) forming a polysilicon line on said substrate, said polysilicon line having sidewalls;

(c) forming an insulating sidewall layer on said sidewalls of said polysilicon line;

(d) removing a portion of said polysilicon line and a corresponding portion of said insulating sidewall layer in a contact region of said polysilicon line; and

(e) forming a silicide layer on said sidewall of said polysilicon line in said contact region.

[c2] 2. The method of claim 1, step (d) further including:

simultaneously removing additional sections of said polysilicon line and corresponding sections and said insulating sidewall layer to sever said polysilicon line into gate segments.

[c3] 3. The method of claim 1, wherein said polysilicon line is in the shape of a closed loop.

[c4] 4. The method of claim 1, further including:

between steps (d) and (e) forming a doped silicon region in said substrate; and

said silicide layer extending over and in direct contact with at least a portion of said doped silicon region.

[c5] 5. The method of claim 4, further including:

between steps (a) and (b) forming a gate dielectric on a top surface of

said substrate.

[c6] 6. The method of claim 1, wherein said silicide layer is selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide and platinum silicide.

[c7] 7. The method of claim 1, further including:
forming another silicide layer on said top surface of said polysilicon line.

[c8] 8. The method of claim 7, wherein said another silicide layer includes a material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide and platinum silicide.

[c9] 9. The method of claim 1, wherein said polysilicon line is doped N-type or P-type.

[c10] 10. The method of claim 1, wherein said polysilicon line in said contact region has a width less than said polysilicon line in regions of said polysilicon line immediately adjacent to said contact region.

[c11] 11. The method of claim 1, further including:
between steps (b) and (c) forming an insulating capping layer over a top surface of said polysilicon line; and
step (d) including simultaneously removing corresponding sections of said insulating capping layer in said contact region of said polysilicon line;

[c12] 12. A method of fabricating a static random access memory (SRAM) cell; comprising:
(a) providing a substrate and forming a dielectric layer on a top surface of said substrate;
(b) forming a polysilicon line on a top surface of said dielectric layer;
(c) forming an insulating layer on said sidewalls of said first and second

gates segments;

(d) removing segments of said polysilicon line and corresponding portions of said insulating layer to form a first gate segment common to said first PFET and said first NFET and a second gate segment common to said second PFET and said second NFET, said first and second gate segments having top surfaces, sidewalls and ends;

(e) forming source and drains of a first PFET, a second PFET, a first NFET, second NFET, a third NFET and a fourth NFET in said substrate;

(f) forming a first silicide layer contacting a first of said ends of said first gate segment and a drain of said second PFET;

(g) forming a second silicide region contacting a contact region of at least one said sidewalls of said second gate segment and a drain of said first PFET;

(h) forming a third silicide region contacting a contact region of at least one said sidewalls of said first gate segment and a drain of said second NFET;

(i) forming a fourth silicide region contacting a first end of said ends of said second gate segment, a drain of said first PFET and a drain of said fourth NFET; and

(j) forming a fifth silicide region contacting a second end of said ends of said first gate segment and a drain of said third NFET.

[c13] 13. The method of claim 12, step (d) further including:

removing a first partial section of said polysilicon line and a corresponding portion of said sidewall layer to form said contact region of at least one sidewall of said sidewalls of said first gate segment, said first partial section insufficient to completely sever said first gate segment; and

removing a second partial section of said polysilicon line and a

corresponding portion of said sidewall layer to form said contact region of at least one sidewall of said sidewalls of said second gate segment, said second partial section insufficient to completely sever said second gate segment.

[c14] 14. The method of claim 12,
step (c) further including: forming an insulating capping layer over said top surfaces of said first and second gate segments; and
step (d) further including: removing a corresponding portion of said insulating capping layer in said contact region of at least one sidewall of said sidewalls of said first gate segment and removing a corresponding portion of said insulating capping layer in said contact region of at least one sidewall of said sidewalls of said second gate segment.

[c15] 15. The method of claim 12, wherein:
a width of said first gate segment in said contact region of at least one said sidewall of said first gate segment is less than a width of said first gate segment in regions of said first gate segment immediately adjacent to said contact region of at least one said sidewalls of said first gate segment;
a width of said second gate segment in said contact region of at least one said sidewall of said second gate segment is less than a width of said second gate segment in regions of said second gate segment immediately adjacent to said contact region of at least one said sidewalls of said second gate segment.

[c16] 16. The method of claim 12, wherein:
step (b) is performed after step (a); step (c) is performed after step (b), step (d) is performed after step (c), step (e) is performed after step (d), step (f) is performed after step (e), step (f) is performed after step (e),

step (g) is performed after step (f); step (h) is performed after step (g), step (i) is performed after step (h) and step (j) is performed after step (i).

[c17] 17. The method of claim 16, further including:
forming a sixth silicide region on said top surfaces of said first and second gates segments and under said insulating capping layer.

[c18] 18. The method of claim 12, wherein:
step (d) includes forming a third gate segment; and
further including forming contacts to the sources of said first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET, at least one of said contacts overlapping either said first gate segment, said second gate segment or a third gate segment and overlapping one of said sources of said first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET, said at least one of said contacts in electrical contact to one of one of said sources of said first PFET, secondPFET, first NFET, second NFET, third NFET and fourth NFET but not in electrical contact with said first gate segment, said second gate segment and said third gate segment.

[c19] 19. A structure, comprising:
a polysilicon line on a substrate, said polysilicon line having a sidewall;
an insulating sidewall layer on said sidewall of said polysilicon line except in a contact region of said polysilicon line, said contact region extending into said polysilicon line, said polysilicon line in said contact region having a width less than said a width of said polysilicon line in regions of said polysilicon line immediately adjacent to said contact region; and
a silicide layer on said sidewall of said polysilicon line in said contact region.

[c20] 20. The structure of claim 19, further including:
a silicon region in said substrate; and
said silicide layer extending over and in direct contact with at least a portion of said silicon region.

[c21] 21. The structure of claim 20, further including:
a gate dielectric between said polysilicon line and a top surface of said substrate.

[c22] 22. The structure of claim 19, wherein said silicide layer includes a material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide and platinum silicide.

[c23] 23. The structure of claim 19, further including:
another silicide layer on said top surface of said polysilicon line.

[c24] 24. The structure of claim 23, wherein said another silicide layer includes a material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide and platinum silicide.

[c25] 25. The structure of claim 19, wherein said polysilicon line is doped N-type or P-type.

[c26] 26. The structure of claim 19, further including:
an insulating capping layer over a top surface of said polysilicon line.

[c27] 27. A static random access memory (SRAM) cell; comprising:
a first PFET, a second PFET, a first NFET, a second NFET, a third NFET and a fourth NFET, each PFET and NFET having a source and a drain;
a first gate segment common to said first PFET and said first NFET and a second gate segment common to said second PFET and said second NFET, said first and second gate segments having top surfaces,

sidewalls and ends;

a first silicide layer contacting a first of said ends of said first gate segment and a drain of said second PFET;

a second silicide layer contacting a contact region of at least one said sidewalls of said second gate segment and a drain of said first PFET;

a third silicide layer contacting a contact region of at least one said sidewalls of said first gate segment and a drain of said second NFET;

a fourth silicide layer contacting a first end of said ends of said second gate segment, a drain of said first PFET and a drain of said fourth NFET; and

a fifth silicide layer contacting a second end of said ends of said first gate segment and a drain of said third NFET.

[c28] 28. The SRAM cell of claim 27, wherein said sidewalls of said first and second gate segments are covered by an insulating layer except in said contact region of at least one of said sidewalls of said first gate segment and said contact region of at least one of said sidewalls of said second gate segment.

[c29] 29. The SRAM cell of claim 27, wherein:

a width of said first gate segment in said contact region of at least one said sidewall of said first gate segment is less than a width of said first gate segment in regions of said first gate segment immediately adjacent to said contact region of at least one said sidewalls of said first gate segment;

a width of said second gate segment in said contact region of at least one said sidewall of said second gate segment is less than a width of said second gate segment in regions of said second gate segment immediately adjacent to said contact region of at least one said sidewalls

of said second gate segment.

[c30] 30. The SRAM cell of claim 27, further including:
an insulating capping layer over said top surfaces of said first and second gate segments; and
an insulating sidewall layer over said sidewalls of said first and second gate segments except in (a) said contact region of at least one said sidewall of said first gate segment, (b) said contact region of at least one said sidewall of said second gate segment and (c) said ends of said first and second gate segments.

[c31] 31. The SRAM cell of claim 30, further including:
a sixth silicide layer on said top surfaces of said first and second gates segments and under said insulating capping layer.

[c32] 32. The SRAM cell of claim 30, further including:
contacts to the sources of said first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET, at least one of said contacts overlapping either said first gate segment, said second gate segment or a third gate segment and overlapping one of said sources of first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET, said at least one of said contacts in electrical contact to one of said sources of said first PFET, second PFET, first NFET, second NFET, third NFET and fourth NFET but not in electrical contact with said first gate segment, said second gate segment and said third segment.